LF2272
Colorspace Converter/ Corrector (3 x 12-bits)

FEATURES

- 50 MHz Data and Computation Rate
- Full Precision Internal Calculations with Output Rounding
- On-board 10-bit Coefficient Storage
- Overflow Capability in Low Resolution Applications
- Two's Complement Input and Output Data Format
- 3 Simultaneous 12-bit Channels (64 Giga Colors)
- Applications:
  - Component Color Standards Translations (RGB, YIQ, YUV)
  - Color-Temperature Conversion
  - Image Capturing and Manipulation
  - Composite Color Encoding/ Decoding
  - Three-Dimensional Perspective Translation
- Replaces TRW/Raytheon/Fairchild TMC2272
- 120-pin PQFP

DESCRIPTION

The **LF2272** is a high-speed digital colorspace converter/corrector consisting of three simultaneous 12-bit input and output channels for functionality up to 64 Giga (2^{36}) colors. Some of the applications the LF2272 can be used for include phosphor colorimetry correction, image capturing and manipulation, composite color encoding/decoding, color matching, and composite color standards conversion/transcoding.

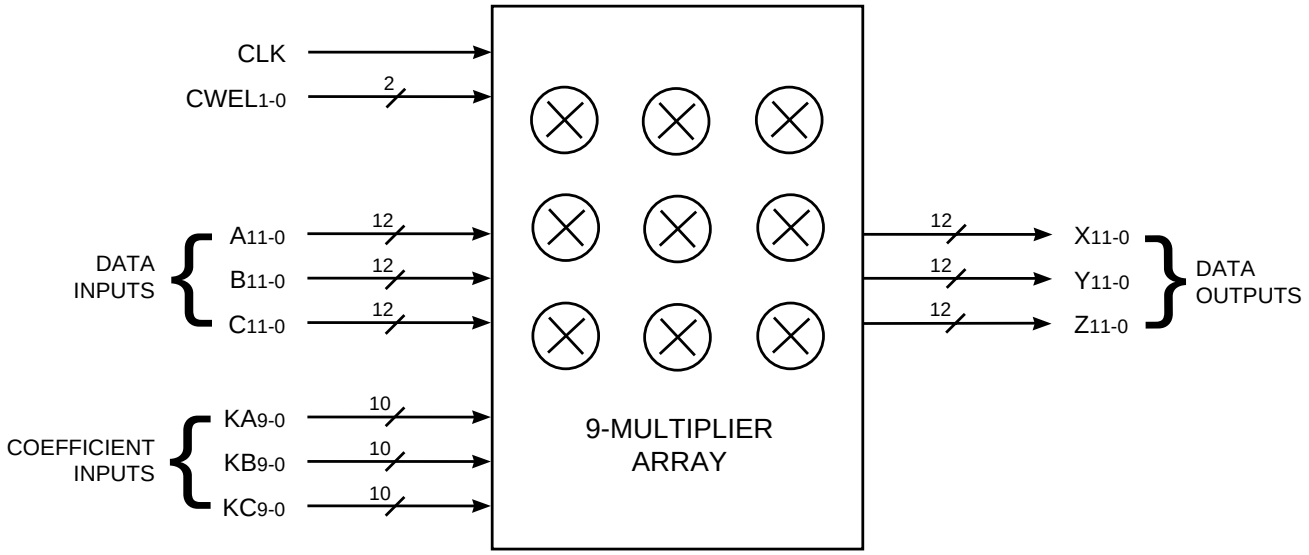
The 3 x 3 matrix multiplier (triple dot product) allows users to easily perform three-dimensional perspective translations or video format conversions at real-time video rates. By using the LF2272, conversions can be made from the RGB (color component) format to the YIQ (quadrature encoded chrominance) or YUV (color difference) formats and vice versa (YIQ or YUV to RGB). Differing signal formats in each stage of a system can be disregarded. For example, using an LF2272 at each format interface allows each stage of a system to operate on the data while in the appropriate format.

All inputs and outputs, as well as all control lines, are registered on the rising edge of clock. The LF2272 operates at clock rates up to 50 MHz over the full commercial temperature and supply voltage ranges. A narrower data path can be used to allow the LF2272 to work with many different imaging applications.

DETAILS OF OPERATION

All three input ports (A, B, C) and all three output ports (X, Y, Z) are utilized to implement a 3 x 3 matrix multiplication (triple dot product). Each truncated 12-bit output is the sum of all three input words multiplied by the appropriate coefficients (Table 1). The pipeline latency is five clock cycles. Therefore, the sum of

LF2272 BLOCK DIAGRAM



products will be output five clock cycles after the input data has been registered. New output data is subsequently available every clock cycle thereafter.

DATA FORMATTING

The data input ports (A, B, C) and data output ports (X, Y, Z) are 12-bit integer two's complement format.

The coefficient input ports (KA, KB, KC) are 10-bit fractional two's complement format. Refer to Figures 1a and 1b.

BIT WEIGHTING

The internal sum of products of the LF2272 can grow to 23 bits. However, in order to keep the output format identical to the input format, the X, Y, and Z outputs are rounded to 12-bit integer words. The rounding is done only at the final output stage to allow accuracy, with correct rounding and overflow, for applications requiring less than 12-bit integer words. The user may adjust the bit weighting by applying an identical scaling correction factor to both the input and output data streams.

TABLE 1. LATENCY EQUATIONS

$$X(n+4) = A(n)KA1(n) + B(n)KB1(n) + C(n)KC1(n)$$
$$Y(n+4) = A(n)KA2(n) + B(n)KB2(n) + C(n)KC2(n)$$
$$Z(n+4) = A(n)KA3(n) + B(n)KB3(n) + C(n)KC3(n)$$

DATA OVERFLOW

Because the LF2272's matched input and output data formats accommodate unity gain (0 dB), input conditions that could lead to numeric overflow may exist. To ensure that no overflow conditions occur, the user must be aware of the maximum input data and coefficient word sizes allowable for each specific algorithm being performed.

SYSTEMS SMALLER THAN 12-BITS

Using a data path less than 12-bits requires the input data to be right justified and sign extended to 12-bits because the LF2272 carries out all calculations to full precision. Since all least-significant bits are used, the desired X, Y, and Z outputs are rounded correctly and upper-order output bits are used for overflow.

FIGURE 1A. INPUT FORMATS

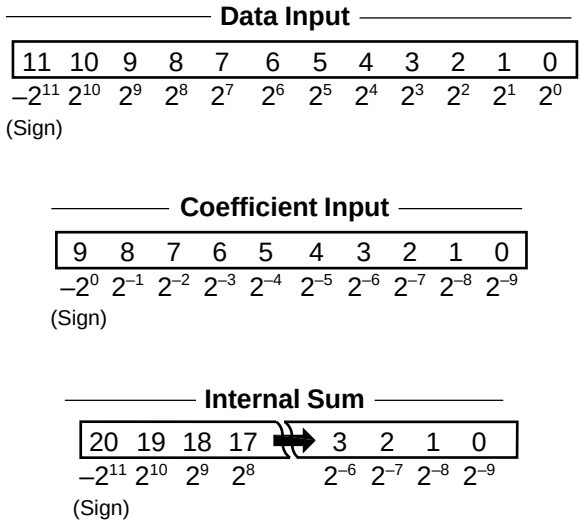
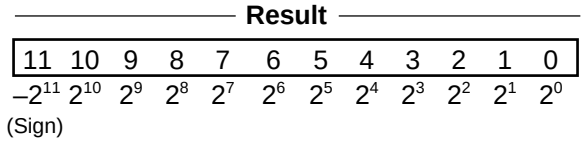


FIGURE 1B. OUTPUT FORMAT



SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

A11-0, B11-0, C11-0 — Data Inputs

A, B, and C are the 12-bit registered data input ports. Data presented to these ports is latched into the multiplier input registers.

KA9-0, KB9-0, KC9-0 — Coefficient Inputs

KA, KB, and KC are the 10-bit registered coefficient input ports. Data presented to these ports is latched into the corresponding internal coefficient register set defined by CWEL1-0 (Table 3) on the next rising edge of CLK. Table 2 shows which coefficient registers are available for each coefficient input port.

TABLE 2. COEFFICIENT INPUTS

INPUT PORT	REG. AVAILABLE
KA	KA1, KA2, KA3
KB	KB1, KB2, KB3
KC	KC1, KC2, KC3

Outputs

X11-0, Y11-0, Z11-0 — Data Outputs

X, Y, and Z are the 12-bit registered data output ports.

Controls

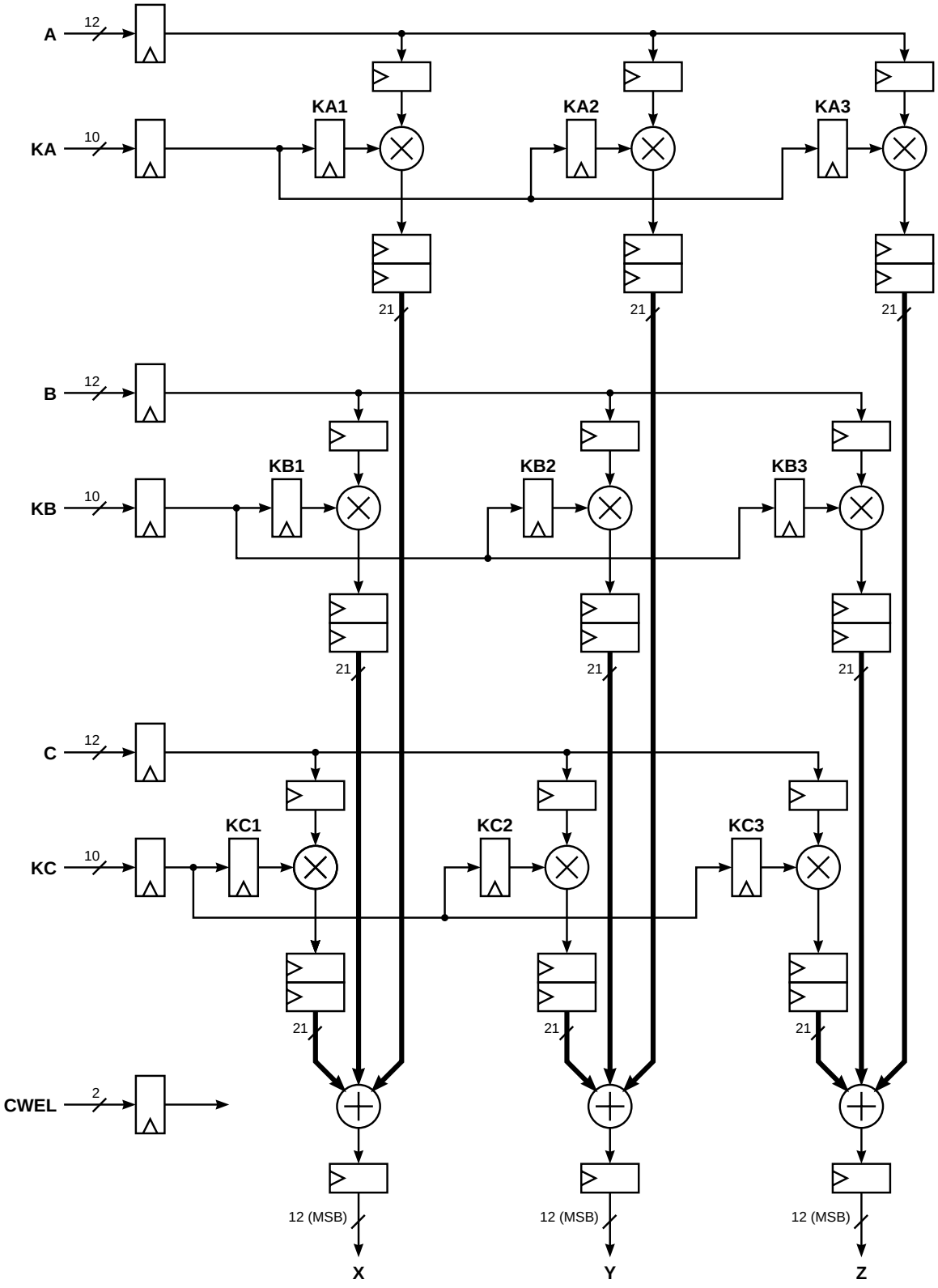
CWEL1-0 — Coefficient Write Enable

The registered coefficient write enable inputs determine which internal coefficient register set to update (Table 3) on the next clock cycle.

TABLE 3. COEFF. REG. UPDATE

CWEL1-0	COEFFICIENT SET
00	Hold All Registers
01	KA1, KB1, KC1
10	KA2, KB2, KC2
11	KA3, KB3, KC3

FIGURE 2. DETAILED FUNCTIONAL DIAGRAM



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
VCC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –0.5 V to VCC + 0.5 V
Signal applied to high impedance output ..... –0.5 V to VCC + 0.5 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	**Temperature Range** (Ambient)	**Supply Voltage**
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ **V**CC ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ **V**CC ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	**V**cc = Min., **I**OH = –2.0 mA	2.4			V
VOL	Output Low Voltage	**V**cc = Min., **I**OL = 4.0 mA			0.4	V
VIH	Input High Voltage		2.0		**V**CC	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ **V**IN ≤ **V**CC (Note 12)			±10	µA
IOZ	Output Leakage Current	(Note 12)			±40	µA
ICC1	**V**CC Current, Dynamic	(Notes 5, 6)			160	mA
ICC2	**V**CC Current, Quiescent	(Note 7)			12	mA
CIN	Input Capacitance	**T**A = 25°C, f = 1 MHz			10	pF
COUT	Output Capacitance	**T**A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

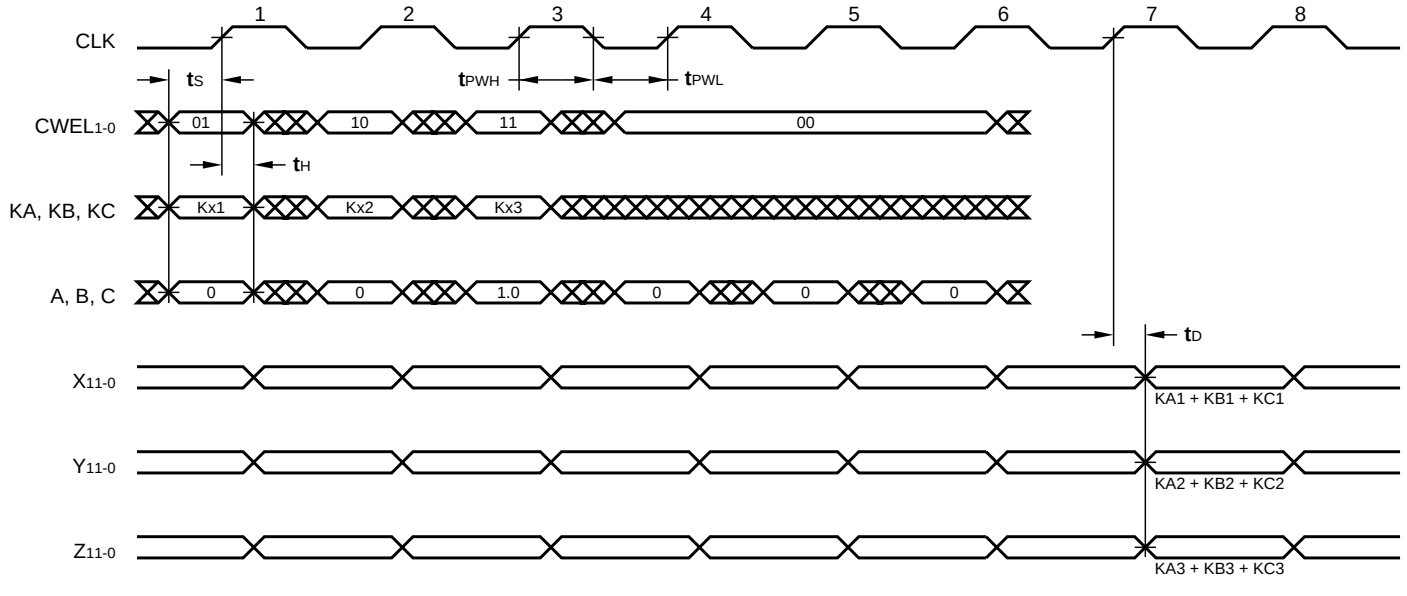
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2272–					
		33*		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25		20	
t_{PWL}	Clock Pulse Width Low	15		10		6	
t_{PWH}	Clock Pulse Width High	10		10		8	
t_S	Input Setup Time	8		6		6	
t_H	Input Hold Time	0		0		0	
t_D	Output Delay		18		16		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF2272–			
		33*		25*	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25	
t_{PWL}	Clock Pulse Width Low	15		10	
t_{PWH}	Clock Pulse Width High	10		10	
t_S	Input Setup Time	12		9	
t_H	Input Hold Time	0		0	
t_D	Output Delay		25		20

SWITCHING WAVEFORM



*DISCONTINUED SPEED GRADE

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

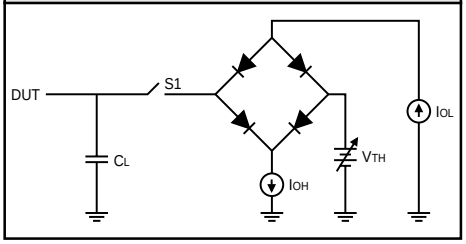
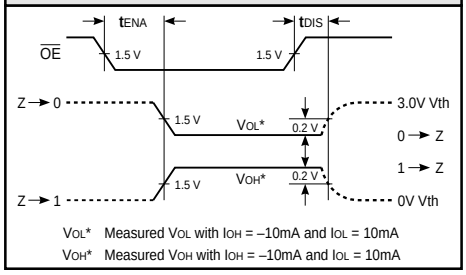
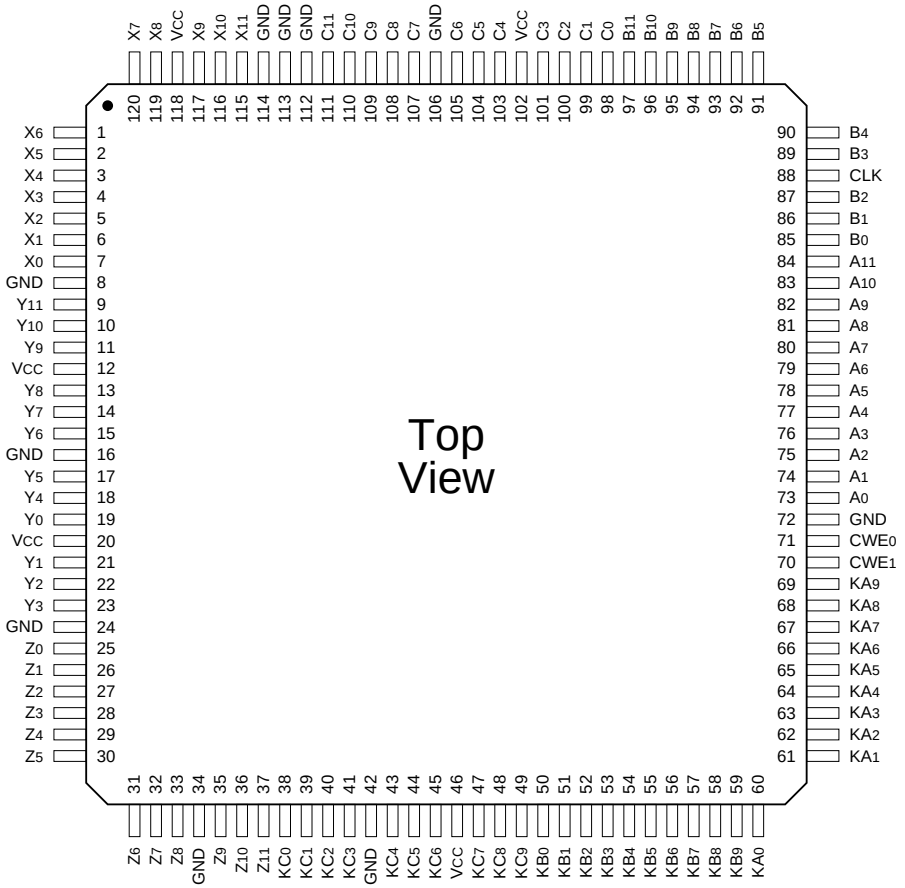


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

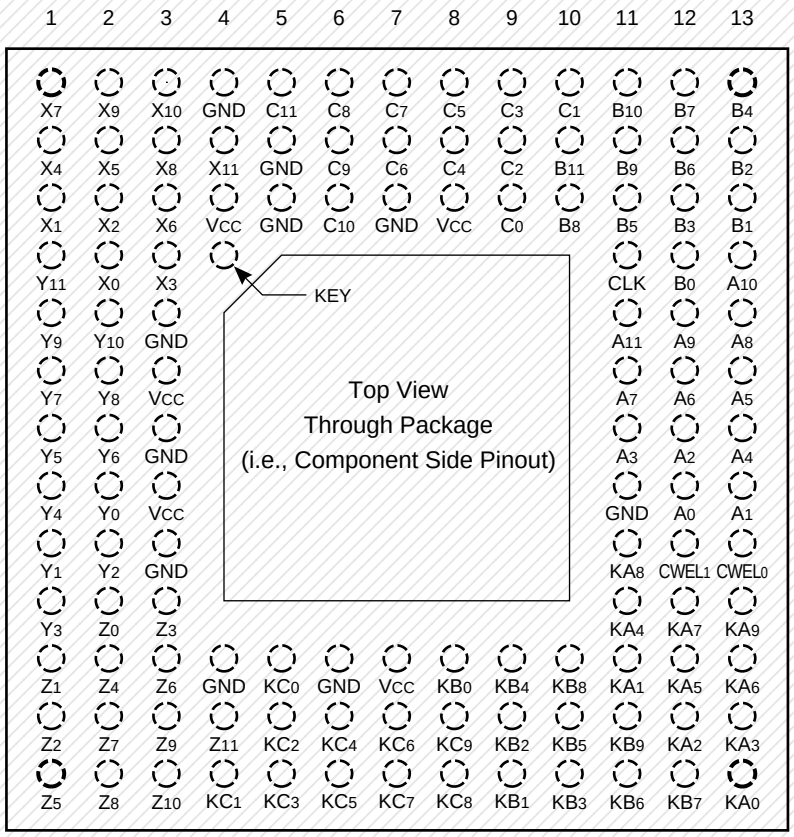
120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C — COMMERCIAL SCREENING
25 ns	LF2272QC25
20 ns	LF2272QC20
	–40°C to +85°C — COMMERCIAL SCREENING

ORDERING INFORMATION

120-pin



Discontinued Package

Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — Commercial Screening
	–55°C to +125°C — Commercial Screening
	–55°C to +125°C — MIL-STD-883 Compliant